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EXAMINER

ROCHE, TRENTON J

ART UNIT

PAPER NUMBER

2124

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/896,780	Applicant(s) COCCA, J. DAVID	
	Examiner Trent J Roche	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is responsive to Amendment A filed 22 July 2004.
2. Claims 1-35 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,412,081 to Koscal et al, hereafter referred to as Koscal.

Regarding claim 1:

Koscal teaches:

- a method for dynamically modifying a stored program (“The patch code is designed to replace the code segment containing the error” in col. 2 lines 48-49)
- storing correction code in at least one of a plurality of correction blocks included in an electrically erasable programmable memory (“memory at which the patch code will reside during execution...the second memory is typically...electronically-erasable programmable ROM (‘EEPROM’)...” in col. 2 lines 26-32)

Art Unit: 2124

- executing a program having instructions stored in the memory (“at least one memory accessible by the processor over a bus system on which is stored a routine which, upon execution thereof by the processor...” in col. 19 lines 55-57. Further, note col. 7 lines 4-6, “the patch code is retained in this second memory, and retrieved and executed by the microprocessor while retained in this memory.” The second memory is the NVRAM, which as stated in col. 6 lines 58-59, “the NVRAM is replaced by EEPROM.”)
- invoking an address match routine to execute at least a portion of the correction code in place of at least one of the instructions during the execution of the program (“causes a patch code segment to be executed in place of an error-containing code segment...” in col. 19 lines 57-59. Further, a matching routine is performed as shown in col. 4 lines 5-8, “if the address stored on the stack is the next sequential address following the patch address, indicating that the interrupt was caused by a trap condition”)
- continuing executing the program after the at least a portion of the correction code executes (“The microprocessor then executes the patch code and, when this has been accomplished, selectively restores context, and returns to an address within the first memory immediately after the program code containing the software error” in col. 4 lines 17-21)

as claimed.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Koscal discloses an address match routine occurring when a program counter associated with the executing of the program matches at least one of a plurality of address match registers as claimed (“if the address stored on the stack is the next sequential address following the patch address, indicating that the interrupt was caused by a

Art Unit: 2124

trap condition...if a trap condition caused the interrupt, the start address of the patch code is retrieved from the predetermined patch address vector, and stored in the program counter..." in col. 4 lines 5-16)

Regarding claim 3:

The rejection of claim 2 is incorporated, and further, Koscal discloses determining for each of the correction blocks whether correction code stored in the blocks is to be executed during the execution of the program, retrieving a first address from the correction code stored in a respective correction block when it is determined that correction code stored in the respective correction block is to be executed, and storing the retrieved first address in one of the plurality of address match registers as claimed ("if the address stored on the stack is the next sequential address following the patch address, indicating that the interrupt was caused by a trap condition...if a trap condition caused the interrupt, the start address of the patch code is retrieved from the predetermined patch address vector, and stored in the program counter..." in col. 4 lines 5-16)

Regarding claim 4:

The rejection of claim 3 is incorporated, and further, Koscal discloses retrieving a first data value from each of the correction blocks having stored correction code, comparing the retrieved first data value from each of the correction blocks having stored correction code to a predetermined value, and determining that the correction code stored in each of the correction blocks is to be executed during program execution when the corresponding first data value equals the predetermined value, otherwise determining that the correction code stored in each of the correction blocks is not to be executed during program execution as claimed ("if the address stored on the stack is the next

Art Unit: 2124

sequential address following the patch address, indicating that the interrupt was caused by a trap condition...if a trap condition caused the interrupt, the start address of the patch code is retrieved from the predetermined patch address vector, and stored in the program counter of the microprocessor. In this fashion, a jump to the patch code is executed.” in col. 4 lines 5-17.)

Regarding claim 5:

The rejection of claim 2 is incorporated, and further, Koscal discloses executing the program in response to a completion of the storing of correction code as claimed (Note at least Figure 4 and the corresponding sections of the disclosure)

Regarding claim 6:

The rejection of claim 2 is incorporated, and further, Koscal discloses saving a plurality of registers and the program counter upon the invoking of the address match routine, retrieving a second data value from each of the correction blocks, comparing the retrieved second data value from each of the correction blocks to a post address match value of the program counter, and identifying the correction block corresponding to the invoking of the address match routine as claimed (Note at least Figure 5 and the corresponding sections of the disclosure.)

Regarding claim 7:

The rejection of claim 6 is incorporated, and further, Koscal discloses branching to an error processing routine as claimed (Note at least Figure 5, item 504 and the corresponding section of the disclosure.)

Art Unit: 2124

Regarding claim 8:

The rejection of claim 6 is incorporated, and further, Koscal discloses a second data value being equal to the value stored in the address match register as claimed (“the processor status register (“PSR”) is read, and a determination made whether the predetermined bit of the PSR is in the second predefined state...” in col. 12 lines 45-48)

Regarding claim 9:

The rejection of claim 6 is incorporated, and further, Koscal discloses an offset value being dependent upon a next program instruction to be executed as claimed (“the microprocessor accesses this vector to obtain the starting address of the interrupt service routine, and loads this starting address into the PC” in col. 9 lines 20-23. The address stored in the PC is inherently dependent on the next program instruction.)

Regarding claim 10:

The rejection of claim 6 is incorporated, and further, Koscal discloses retrieving a third address identifying a return address, restoring the plurality of registered, branching the executing of the program to the third address, and executing the program as claimed (“First the context of the microprocessor is optionally saved...The microprocessor then executes the patch code and, when this has been accomplished, selectively restores context, and returns to an address within the first memory immediately after the program code containing the software error” in col. 4 lines 2-21)

Regarding claim 11:

Art Unit: 2124

The rejection of claim 1 is incorporated, and further, Koscal discloses an address match interrupt service routine having a corresponding address match interrupt entry in a vector table as claimed (“if a trap condition caused the interrupt, the start address of the patch code is retrieved from the predetermined patch address vector, and stored in the program counter of the microprocessor. In this fashion, a jump to the patch code is executed.” in col. 4 lines 13-17.)

Regarding claim 12:

The rejection of claim 1 is incorporated, and further, Koscal discloses retrieving a second address from the correction code identifying a starting address, branching the executing of the program to the second address, and executing the at least a portion of the correction code beginning at the second address as claimed (“if a trap condition caused the interrupt, the start address of the patch code is retrieved from the predetermined patch address vector, and stored in the program counter of the microprocessor. In this fashion, a jump to the patch code is executed.” in col. 4 lines 13-17.)

Regarding claim 13:

The rejection of claim 1 is incorporated, and further, Koscal discloses instructions for continuing executing the program after the at least a portion of the correction code executes as claimed (“The microprocessor then executes the patch code and, when this has been accomplished, selectively restores context, and returns to an address within the first memory immediately after the program code containing the software error” in col. 4 lines 17-21)

Regarding claim 14:

Art Unit: 2124

The rejection of claim 1 is incorporated, and further, Koscal discloses selecting at least one of the plurality of correction blocks for storing the correction code, erasing the selected block, and transferring the correction code from an external source to the selected correction block as claimed (“this data structure represents data that is provided in a second memory...an OEM stores this data in the second memory along with program code or data needed to provide additional features and functions to an electronic device...” in col. 10 lines 18-23)

Regarding claim 15:

The rejection of claim 14 is incorporated, and further, Koscal discloses correction code transferred from the external source by at least one of a wired and wireless connection as claimed (“these functions or features are provided to the device from a remote location through a telecommunications link to a second memory...The telecommunications link may comprise a wireless link...” in col. 10 lines 35-39)

Regarding claim 16:

The rejection of claim 1 is incorporated, and further, Koscal discloses the step of storing correction code in at least one of a plurality of correction blocks in response to at least one of a detection that an external source is coupled to the memory and an invocation of a periodically scheduled maintenance routine as claimed (“these functions or features are provided to the device from a remote location through a telecommunications link to a second memory... in col. 10 lines 35-37. The remote location is coupled to the second memory through the link.)

Regarding claims 17-32:

Art Unit: 2124

Claims 17-32 are directed to a micro-controller for performing the methods of claims 1-16, respectively, and are rejected for the reasons set forth in connection with claims 1-16, respectively.

Regarding claim 33:

The rejection of claim 17 is incorporated, and further, Koscal discloses the electrically erasable programmable memory being included on the same electronic chip as the remaining logic comprising the micro-controller as claimed (Note Figure 1 and the corresponding section of the disclosure.)

Regarding claim 34:

Koscal teaches:

- an electrically erasable programmable memory based memory map structure supporting an address match interrupt scheme (“memory at which the patch code will reside during execution...the second memory is typically...electronically-erasable programmable ROM (‘EEPROM’)...” in col. 2 lines 26-32. Further, this supports an address match interrupt scheme, as shown in col. 4 lines 5-8, “if the address stored on the stack is the next sequential address following the patch address, indicating that the interrupt was caused...”)
- a random access memory (RAM) area including a program stack for temporarily storing program information (Note Figure 1, item 110 and the corresponding section of the disclosure.)
- a main program area for storing at least one executable program (Note Figure 1, item 108 and the corresponding section of the disclosure.)

Art Unit: 2124

- an initialization area for storing code to enable an address match interrupt for at least one of the correction blocks (Note Figure 1, item 142 and the corresponding section of the disclosure.)
- a special function register (SFR) area including a plurality of address interrupt registers (“a predetermined bit in the processor status register...” in col. 3 lines 12-13)
- a vector table for triggering the address match interrupt when a program counter associated with the at least one executable program matches a register value stored in one of the plurality of address interrupt registers (“if the address stored on the stack is the next sequential address following the patch address, indicating that the interrupt was caused...” in col. 4 lines 5-8. Further, note Figure 3, item 302 and the corresponding section of the disclosure.)
- an interrupt service routine (ISR) area including an address match ISR (“if the address stored on the stack is the next sequential address following the patch address, indicating that the interrupt was caused...” in col. 4 lines 5-8)
- wherein the address match ISR identifies which one of the plurality of correction blocks corresponds to the triggering of the address match interrupt to execute at least a portion of the correction code in place of at least one instruction of the at least one executable program during program execution (Note at least Figure 5 and the corresponding sections of the disclosure.)

substantially as claimed.

Regarding claim 35:

Art Unit: 2124

The rejection of claim 34 is incorporated, and further, Koscal discloses a first data value, a second data value, a first address, a second address, and a third address as claimed (Note at least Figure 10 and the corresponding section of the disclosure.)

Response to Arguments

5. Applicant's arguments filed 22 July 2004 have been fully considered but they are not persuasive.

Per claim 1:

The applicant states that "Nowhere does Koscal disclose the program to be corrected and the patch code are stored in the same memory, much less the same electrically erasable programmable memory, as claim 1 requires." In response, it is noted that the language of claim 1 does not require what the applicant states above. Rather, claim 1 recites "storing correction code in at least one of a plurality of correction blocks included in an electrically erasable programmable memory; executing *a program having instructions* (emphasis added) stored in the memory..." There is no language recited in the claim that states the program to be corrected and the patch code being in the same memory, much less the same electrically erasable programmable memory; only that correction code is stored in the electrically erasable programmable memory, and further, *a program having instructions* (emphasis added) is also stored in the same electrically erasable programmable memory. As shown in the rejection regarding claim 1, the patch code is stored in a second memory, and "the patch code is retrieved and executed by the microprocessor while retained in this memory." (col. 7 lines 5-6) As such, Koscal does disclose storing correction code in at least one of a plurality of correction blocks

Art Unit: 2124

included in an electrically erasable programmable memory, and executing a program having instructions stored in the memory, as required by claim 1.

Further, the applicant states that Koscal does not disclose a plurality of correction blocks as recited in claim 1. In response, it is noted that claim 1 requires only "at least one of a plurality of correction blocks included in an electrically erasable programmable memory." As such, it is required to only show *at least one* correction block. Furthermore, memory is made up of blocks which contain data (Note "Efficient Memory Programming, page 32, section titled Data Blocking). When the invention disclosed by Koscal writes the patch code to the electrically erasable programmable memory, the patch code is inherently stored in blocks in the memory. These blocks, containing correction code from the patch, are "correction blocks" according to the broadest reasonable interpretation of the claim. As such, Koscal discloses at least one of a plurality of correction blocks as required by claim 1.

For these reasons, the rejection of claim 1 is proper and maintained.

Per claim 4:

The applicant states that Koscal does not describe retrieving of a first data value from each of the correction blocks having stored correction code. In response, it is noted that Koscal is comparing a program address to an address corresponding to the patch code in memory. As such, the invention disclosed by Koscal is inherently going to have to retrieve a data value from the correction blocks corresponding to the patch code in order to compare the addresses, as even an address represents a data value. As such, Koscal does disclose retrieving a first data value from the correction blocks

Art Unit: 2124

having correction code stored thereon, and for this reason, the rejection of claim 4 is proper and maintained.

Per claims 6-10:

The applicant states that Koscal does not describe retrieving a second data value from each of the correction blocks having stored correction code, comparing the retrieved second data value from each of the correction blocks having stored correction code to a post address match value of the program counter, and identifying the correction block corresponding to the invoking of the address match routine as the correction block having the second data value equal to the post address match value of the program counter. The applicant further states that nothing in Koscal discloses “retrieving a second data value from each of the correction blocks and then comparing this retrieved value with a post address match value of the program counter, e.g., a value after the correction code stored in one (of) the correction blocks has been executed.” In response, it is noted that nothing in the claim recites that the post address match value is the program value which occurs after execution of the correction code; only that once an address match routine is invoked, a plurality of registers and the program counter are saved. Furthermore, as claim 6 is dependent on claim 2, and claim 2 does not recite what a first data value may be, the aspect of a second data value is interpreted to be a first comparison of data values. In col. 13 lines 3-6, Koscal states “comparing the contents of the PC stored on the stack in step 515 with the patch address to determine if the address stored on the stack is the next sequential location following the patch address.” The contents of the PC on the stack are compared to the data value from the patch code, and the comparison occurs after (post) step 504 in Figure 5. As such, Koscal discloses the limitations required by claim 6, and as such, the rejections of claim 6-10 are proper and maintained.

Art Unit: 2124

Per claims 2, 3, 5 and 17-35:

The applicant states that claims 2, 3, 5 and 17-35 are allowable for the reasons given in connection with claims 1, 4 and 6-10. As was shown above, the rejections of claim 1, 4 and 6-10 are proper and maintained, and as such, the argument that claims 2, 3, 5 and 17-35 are allowable is considered moot, and the rejections of claim 2, 3, 5 and 17-35 are proper and maintained.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (703)305-4627. The examiner can normally be reached on Monday - Friday, 9:00 am - 5:30 pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2124

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trent J Roche
Examiner
Art Unit 2124

TJR


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